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Sequential Multiplier

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**Sequential Multiplier using Booth’s Algorithm**

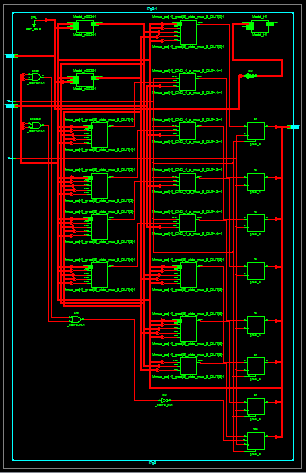
# Design Approach:

Sequential Multiplier is an electronic circuit used in digital electronics, to multiply two binary numbers. It is built using binary adder and other possible sequential circuits. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of partial products, and then summing the partial products together.

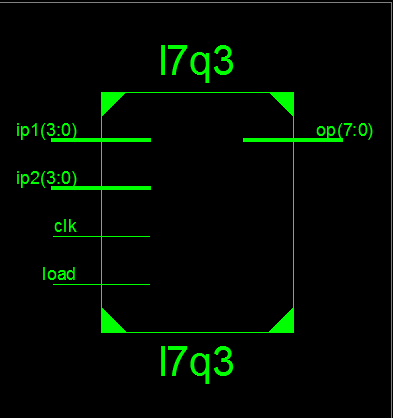
We have implemented the booths algorithm that performs multiplication in various steps. For this, we have taken one 9 bit register. Its last bit is 0 initially. Depending upon last bit of input and our initial value, we have performed 4 cases using case statement. If MSB of IP1 is one implies that it is negative number, so we have loaded 2’s complement of input. Additionally, we have taken one counter and the value of counter will be 4, when output will be valid.

**Synthesis:**

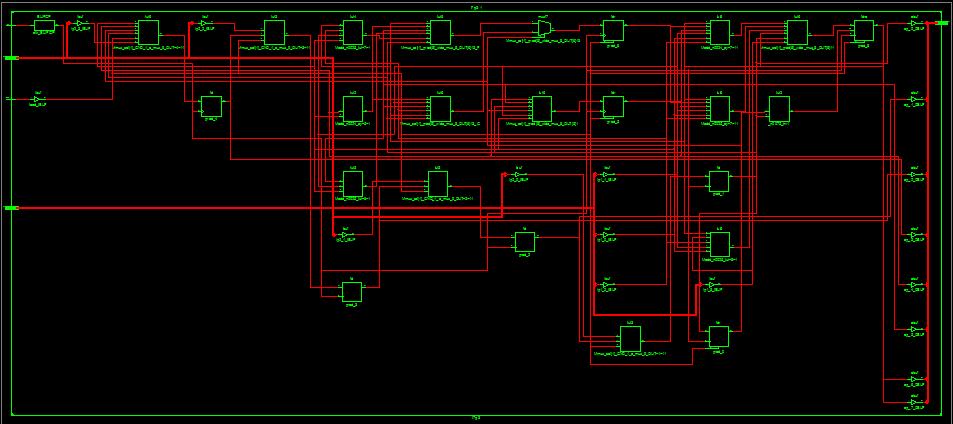
1. RTL Schematic



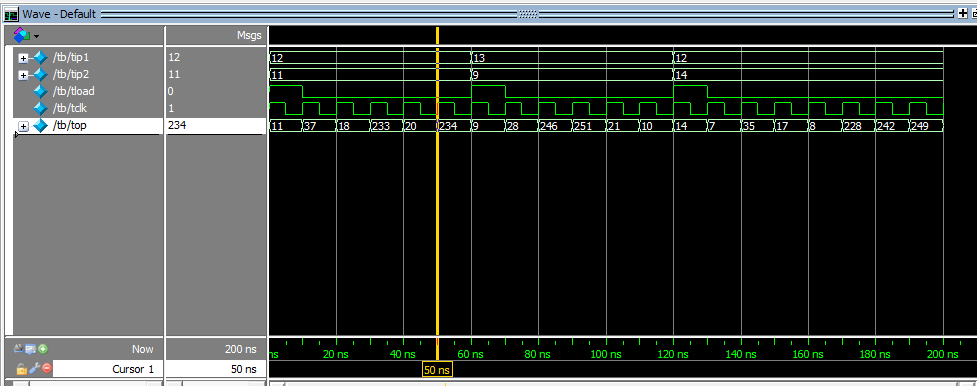
1. Block Diagram

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1. Tech Schematic



1. Simulation Waveform Result

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**Error:**

None

**Verified by:**

Dharamvir Chundawat (150240133007)